DATA RECOVERY SYSTEM AND THE METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a data recovery system and method and, more particularly, to a system and method for recovering data in a serial transmission.

2. Description of Related Art

When serial data in a high-speed serial transmission is sampled, it will incur clock skew because the phase of a recovered clock for sampling serial data has a different phase to that of sampled serial data. A direct solution is to oversample the serial data such that the clock skew can be eliminated by increasing the sampling frequency. U.S. Patent No. 5,905,769 disclosed an oversample-based solution for eliminating clock skew caused by sampling serial data. The conventional method is to correct data of a current sampling data window by using a phase signal of the preceding sampling data window. However, the conventional method cannot do a real-time correction. Particularly, when the phase change caused by clock skew only occurs on the current sampling data window, not only the real-time correction is impossible but an error can be easily caused. Therefore, it is desirable to provide an improved system and method to mitigate and/or obviate the aforementioned problems.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a data recovery system and the method thereof for obviating clock skew.

Another object of the present invention is to provide a data recovery system and the method thereof for real-time correcting clock skew in serial transmission.

To achieve the objects, the data recovery system of the present invention includes: an oversampler, which oversamples an input signal by n-time frequency; a phase detection circuit, which receives the oversampled signals and outputs a phase signal according to a plurality of transitions of the oversampled signals;; a data pick circuit, which receives a phase signal detected by the phase detection circuit and accordingly divides the oversampled signals into n groups to pick one with m-bit data as an output; a data overlap/skip detection circuit, which determines if data is overlapped or skipped according to a relation between the phase signal and a last phase signal; and a data correction circuit, which corrects data when data is overlapped or skipped.

To achieve the objects, the data recovery method of the present invention includes: an oversampling step, which oversamples a received data signal by n-time frequency and thus generates a series of oversampled signals; a picking step, which picks an (nk+1)-bit oversampled signal from the series of oversampled signals; a transition detecting step, which detects nk transitions of the (nk+1)-bit oversampled signal and thus outputs an nk transition signal; a selecting step, which divides the transition signal into n groups, selects one with the maximum transitions from the n groups and outputs a phase signal; a data picking step, which divides the series of oversampled signals into n groups of output data, and outputs one with

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m-bit output data from the n groups according to the phase signal; an overlap/skip detecting step, which receives the phase signal and outputs a status according to a combination of the phase signal and a last phase signal; and a data correcting step, which picks (m+1)-, m-, or (m-1)-bit data

5   selected from both the m-bit output data in the series of oversampled signals and a last oversampled signal at last time for data correction according to the status, and thus outputs an m-bit accurate data.

Other objects, advantages, and novel features of the invention will become more apparent from the following detailed description when taken

10   in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the present invention;

FIG. 2 is a sampling timing of an oversampler of the present invention;

15   FIG. 3 is a circuit of a phase detection circuit of the present invention;

FIG. 4 is a schematic view of a best data sampling point of the present invention;

FIG. 5 is a circuit of a data selection circuit of the present invention;

20   FIG. 6 is a schematic view of data overlap generation of the present invention;

FIG. 7 is a schematic view of data skip generation of the present invention;

FIG. 8 is a view of pseudo codes of a data overlap/skip detection

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circuit of the present invention;

FIG. 9 is a view of pseudo codes of a data correction circuit of the present invention; and

FIG. 10 is a flowchart of a data recovery method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference to FIG. 1, there is shown a preferred embodiment of a data recovery system in accordance with the present invention. In FIG. 1, the data recovery system includes an oversampler 10, a phase detection circuit 20, a data pick circuit 30, a data overlap/skip detection circuit 40 and a data correction circuit 50. The oversampler 10 oversamples each bit of the input signal by a multiplied frequency and groups a plurality of sampled input signals as an oversampled signal output unit. In this embodiment, the oversampler 10 oversamples the input signal by a triple frequency, which means that each bit of the input signal is sampled three times. The input signal is a data with 10 bits. Therefore, the oversampler 10 outputs one oversampled signal unit, which includes 30 oversampled signals, at a time to the phase detection circuit 20 and the data pick circuit 30.

The phase detection circuit 20 detects a plurality of transitions of the oversampled signals and outputs a phase signal. In the embodiment, the phase detection circuit 20 receives the 30 and executes the phase detection according to the oversampled signals of the oversampled signal unit and the last oversampled signal of last oversampled signal unit, which stored internally in the phase detection circuit 20. It should be noted that the last

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oversampled signal of last oversampled signal unit may not be put into consideration for phase detection. In this manner, only parts of the oversampled signals (3n+1, where n=1~9) of the oversampled signal unit are used for phase detection. Accordingly, a phase signal is obtained and

5   sent to the data pick circuit 30 and the data overlap/skip detection circuit 40. The data pick circuit 30 receives the phase signal detected by the phase detection circuit 20 and accordingly divides the oversampled signal output unit into three groups and then choose one of the groups with 10-bit data as an output to the data correction circuit 50. The data overlap/skip detection

10   circuit 40 determines whether data is overlapped or skipped according to the phase signal and the last phase signal received from the phase detection circuit 20, and outputs the result to the data correction circuit 50. According to the result, the data correction circuit 50 chooses either 11-, 10-, or 9-bit data from 11-bit data including both 10-bit data outputted by the data pick

15   circuit 30 and a last oversampled signal of last oversampled signal output unit to execute the data correction, and thereby outputs a 10-bit accurate data.

As shown in the timing diagram of FIG. 2, the oversampler 10 regularly samples input signals by triple sampling frequency in order to

20   obtain 30 oversampled signals S[29:0], wherein S29 is the first oversampled signal while S0 is the last one. When the oversampler 10 accumulates 30 oversampled signals, the signals are sent as an oversampled signal unit to the phase detection circuit 20 and the data pick circuit 30. In addition, S0' is the last oversampled signal of the last oversampled signal

unit and S29" is the first oversampled signal of the next oversampled signal unit.

FIG. 3 shows a circuit diagram of the cited phase detection circuit 20. In FIG. 3, the circuit 20 includes a transition detector 21 and a tally 22. The transition detector 21 includes 30 XOR gates to perform an XOR operation to each of the oversampled signal and the adjacent oversampled signals, thereby detecting a transition. The first oversampled signal is operated XOR with the last oversampled signal S0'. In this manner, there are 30 transitions detected. The 30 transitions are respectively numbered as PA[9:0], PB[9:0] and PC[9:0], where $PAn = S_{3n+2} \oplus S_{3n+3}$, $PBn = S_{3n+1} \oplus S_{3n+2}$, $PCn = S_{3n} \oplus S_{3n+1}$, where $n = 0 \sim 9$. Namely, a transition between S_{3n} and S_{3n+1} is indicated as $PCn = "1"$, a transition between S_{3n+1} and S_{3n+2} (or S_{3n-1}) is indicated as $PBn = "1"$, and a transition between S_{3n+2} (or S_{3n-1}) and S_{3n} is indicated as $PAn = "1"$.

The tally 22 selects one group out of PA[9:0], PB[9:0], and PC[9:0] with the maximum transitions and outputs a phase signal corresponding to the group. One embodiment of the tally 22 is that it includes a maximum selector 225 and three adders 221, 222, 223. Namely, adder 221 adds PA9~PA0 to thus obtain a signal SumA, adder 222 adds PB9~PB0 to obtain a signal SumB, and adder 223 adds PC9~PC0 to obtain a signal SumC. Accordingly, the time of data transition between 0 and 1 can be determined. The value of the signal SumA represents total transition number between S_{3n+2} (or S_{3n-1}) and S_{3n}. The value of the signal SumB represents a total transition number between S_{3n+1} and S_{3n+2} (or S_{3n-1}). The value

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of the signal SumC represents a total transition number between S_{3n} and S_{3n+1}. The maximum selector 225 outputs one phase signal corresponding to the maximum from the outputs of the adders 221, 222 and 223. For example, phase A is outputted if SumA has the maximum value, phase B is outputted if SumB has the maximum value, and phase C is outputted if SumC has the maximum value.

If SumA is the maximum value, it means that the transition between S_{3n+2} (or S_{3n-1}) and S_{3n} happens most compared to S_{3n+1} and S_{3n+2} (or S_{3n-1}), and S_{3n} and S_{3n+1}, as shown in arrow A of FIG.4. In order to obtain the stable and accurate data, the accurate data must be away from the transition when selecting from the oversampled signals. Thus, S_{3n+1} is selected as accurate data, as shown in arrow B of FIG.4.

An embodiment of the maximum selector 225 includes three comparators, comparing two of SumA, SumB and SumC to obtain magnitude relations of (SumA, SumB), (SumB, SumC) and (SumC, SumA) respectively. Another embodiment of maximum selector 225 comprises two comparators, one comparator compares SumA and SumB to obtain the maximum one (A,B)max and another comparator compares the maximum one (A,B)max and SumC. Accordingly, the maximum one in SumA, SumB and SumC is known.

FIG. 5 shows the configuration of the data pick circuit 30. In FIG. 5, the circuit 30 divides the 30 oversampled signals into three groups, $S_{3n+2} = \{S29, S26, ..., S2\}$, $S_{3n+1} = \{S28, S25, ..., S1\}$

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and $S_{3n} = \{S27, S24, \ldots, S0\}$. Upon the phase signal outputted by the phase detection circuit 20, the circuit 30 picks the appropriate one from the three groups as dat[9:0] to output. When the phase signal outputted by the phase detection circuit 20 is 'Phase A', data[9:0] is $S_{3n+1} = \{S28,$

5    $S25, \ldots, S1\}$, i.e., $dat9 = S28$, $dat8 = S25, \ldots, dat0 = S1$. When the phase signal outputted by the phase detection circuit 20 is 'Phase B', data[9:0] is $S_{3n} = \{S27, S24, \ldots, S0\}$. When the phase signal outputted by the phase detection circuit 20 is 'Phase C', data[9:0] is $S_{3n+2} = \{S29, S26, \ldots, S2\}$.

10   Input signals may be delayed or advanced via a transmission channel or cable while the oversampler 10 of the present invention oversamples the input signal by a fixed triple sampling frequency. Such an effect will cause data to overlap or skip. For convenience of description of the data overlap or skip, it is supposed that input signal is 3 bits in a unit and

15   a data window (DW) is defined as 3-bit data. FIG. 6 shows a problem generated by a data overlap phenomenon. In the first data window, the phase signal is 'Phase A' and thus the transition number between S_{3n+2} (or S_{3n-1}) and S_{3n} is the maximum. As shown by arrow A of FIG. 6, in the fixed triple sampling frequency of this embodiment, the best data selecting

20   point is a sampling point with the farthest average distance from A, i.e., at arrow B of FIG. 6.

In the second data window, phase signal is 'Phase B' and thus the transition number between S_{3n+1} and S_{3n+2} (or S_{3n-1}) is the maximum. As shown by arrow C of FIG. 6, the best data selecting point is located at

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arrow D of FIG. 6. In the third data window, the phase signal is 'Phase C' and thus the transition number between S_{3n} and S_{3n+1} is the maximum. As shown by arrow E of FIG. 6, the best data selecting point is located at arrow F of FIG. 6. Based on the phase detection circuit 20 and the data pick circuit 30, oversampled signals T1, T2 in FIG. 6 will be regarded as accurate data to output. However, because the oversampled signals T1, T2 are corresponding to the same data, which means that the same data is oversampled twice, data overlap happens and the overlap signal segment DATA_OL is produced.

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10 FIG. 7 shows a problem generated by a data skip phenomenon. In the first data window, the phase signal is 'Phase A' and thus the transition number between S_{3n+2} (or S_{3n-1}) and S_{3n} is the maximum. As shown by arrow A of FIG. 7, the best data selecting point is a sampling point with the farthest average distance from arrow A, i.e., at arrow B of FIG. 7. In the

15 second data window, the phase signal is 'Phase C' and thus the transition number between S_{3n} and S_{3n+1} is the maximum. As shown in arrow G of FIG. 7, the best data selecting point is located at arrow H of FIG. 7. In the third data window, phase signal is 'Phase B' and thus the transition number between S_{3n+1} and S_{3n+2} (or S_{3n-1}) is the maximum. As shown by

20 arrow I of FIG. 7, the best data selecting point is located at arrow J of FIG. 7. The oversampler 10 oversampled input signal at T3 and T4 but didn't oversample at the time between T3 and T4, at which time the oversampler 10 ought to oversample input signal one more time. Therefore, a oversampled input signal data DATA_SK is generated and a data skip

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phenomenon is caused.

To overcome the cited data overlap/skip phenomenon, the data overlap/skip detection circuit 40 receives the phase signal outputted by the phase detection circuit 20 to determine whether data is overlapped or skipped when the data pick circuit 30 picks data according to the receiving phase signal and the phase signal corresponding to the preceding data window. The circuit 40 then outputs a status, after determination, to the data correction circuit 50. If the phase signal is 'Phase B' in a current data window and 'Phase C' in the preceding data window, data overlap occurs, as shown in FIG. 6. In this case, the status is 'Overlap'. If the phase signal is 'Phase C' in the current data window and 'Phase B' in the preceding data window, data skip occurs, as shown in FIG. 7. In this case, the status is 'Skip'. Otherwise, the status is 'Normal'. The circuit 40 can be implemented by pseudo codes of FIG. 8 created by any hardware description language (HDL) such as Verilog or VHDL.

The data correction circuit 50 picks 11, 10 or 9 bits from both 10-bit data outputted by the data pick circuit 30 and the last oversampled signal S0' for data correction according to the status outputted by the data overlap/skip detection circuit 40, and finally outputs fixed accurate data with 10-bit. When the status is 'Overlap', as shown in FIG. 6, the data correction circuit 50 retains data released by the preceding data window. In this case, because dat9 is presented on the preceding data release, only 9 bit dat[8:0] is released by the current data window for inputting it sequentially to a First In First Out (FIFO) unit. When the status is 'Skip', as shown in

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FIG. 7, the data correction circuit 50 retains data released by the preceding

data window. In this case, the current data window releases both the last

oversampled signal S0' in the preceding data window and the 10 bit dat[9:0],

and inputs them sequentially to a First In First Out (FIFO) unit. Finally, the

5   FIFO unit outputs a 10-bit accurate dat[9:0] sequentially.

The behavior model of the data correction circuit 50 can be

implemented by pseudo codes of FIG. 9 created by any hardware

description language (HDL) such as Verilog or VHDL.

FIG. 10 further shows a flowchart of the data recovery method of the

10   present invention. As shown in FIG. 10, step S301 inputs an input serial

signal. Step S302 (oversampling step) regularly samples the input serial

signal by triple sampling frequency to obtain 30 oversampled signals

S[29:0]. Step S303 (picking step) picks a (30+1)-bit oversampled signals

from a series of oversampled signals, and the (30+1)th-bit oversampled

15   signals are the last oversampled signal S0' of the last oversampled signals

S'[29:0].

Step S304 (transition detecting step) detects 30 transitions of the

(30+1)-bit oversampled signals by performing an XOR operation for each

of the oversampled signal and the adjacent oversampled signals, thereby

20   detecting a transition, and outputs 30 transition signals. The 30 transitions

are divided into three groups PA[9:0], PB[9:0] and PC[9:0], where $PAn = S_{3n+2} \oplus S_{3n+3}$, $PBn = S_{3n+1} \oplus S_{3n+2}$, $PCn = S_{3n} \oplus S_{3n+1}$ and n

$= 0 \sim 9$. Namely, a transition between S_{3n} and S_{3n+1} is indicated as

$PCn = "1"$, a transition between S_{3n+1} and S_{3n+2} (or S_{3n-1}) is indicated

as PBn="1", and a transition between S_{3n+2} (or S_{3n-1}) and S_{3n} is indicated as PAn="1".

Step S305 (selecting step) selects one with the maximum transitions from the three groups PA[9:0], PB[9:0] and PC[9:0], and outputs a phase signal corresponding to the selection. Namely, first, an addition operation is applied to PA9~PA0 for obtaining SumA, to PB9~PB0 for obtaining SumB, and to PC9~PC0 for obtaining SumC. Next, a maximum value is selected from SumA, SumB, and SumC and the phase signal corresponding to the selection is outputted. For example, a phase signal for output is 'Phase A' when SumA has the maximum value, 'Phase B' when SumB has the maximum value, and 'Phase C' when SumC has the maximum value.

Step S306 (data picking step) divides the 30 oversampled signals into three output data $S_{3n+2} = \{S29, S26, ..., S2\}$, $S_{3n+1} = \{S28, S25, ..., S1\}$ and $S_{3n} = \{S27, S24, ..., S0\}$. According to the phase signal output in step S305, an appropriate one in the three groups is selected as 10-bit data dat[9:0] to output. When the phase signal outputted by the phase detection circuit 20 is 'Phase A', data[9:0] is $S_{3n+1} = \{S28, S25, ..., S1\}$, i.e., $dat9 = S28$, $dat8 = S25$, ..., $dat0 = S1$. When the phase signal outputted by the phase detection circuit 20 is 'Phase B', data[9:0] is $S_{3n} = \{S27, S24, ..., S0\}$. When the phase signal outputted by the phase detection circuit 20 is 'Phase C', data[9:0] is $S_{3n+2} = \{S29, S26, ..., S2\}$.

Step S307 (overlap/skip detecting step) receives the phase signal output in step S305 and outputs the overlap/skip detecting signal according

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to the receiving phase signal and the phase signal corresponding to the preceding data window. Namely, if the phase signal is 'Phase B' in a current data window and 'Phase C' in the preceding data window, data overlap occurs. In this case, the status is 'Overlap'. If the phase signal is 'Phase C' in the current data window and 'Phase B' in the preceding data window, data skip occurs. In this case, the status is 'Skip'. Otherwise, the status is 'Normal'.

Step 308 (data correcting step) picks 11, 10 or 9 bits from both the last oversampled signal in the preceding series of oversampled signals and the 10-bit output data for data correction according to the status output in step S307, and thus outputs a 10-bit accurate data dat[9:0].

As aforementioned, the invention can effectively overcome the problem of clock skew in the prior art.

Although the present invention has been explained in relation to its preferred embodiment, it is to be understood that many other possible modifications and variations can be made without departing from the spirit and scope of the invention as hereinafter claimed.